Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claim 1-43 without prejudice.

Please add previously presented claims as follows:

44. (previously presented): A method of forming clusters of processing elements comprising the steps of:

providing a torus array comprising a plurality of processing elements arranged in columns;

shifting the columns of the torus array vertically to form a rhombus;

wrapping the rhombus into a cylinder; and

taking horizontal slices of the cylinder to form clusters of processing elements.

45. (previously presented): An array processor, comprising:

processing elements (PEs) $PE_{i,j}$, where i and j refer to the respective row and column PE positions within a conventional torus-connected array, and where i = 0,1,2, ... N-1 and j = 0, 1, 2, . . . N-1, said PEs arranged in clusters $PE_{(i+a)(ModN),(j+N-a)(ModN)}$, for any i,j and for all $a \in \{0,1,...,N-1\}$; and

cluster switches connected to said clusters providing inter-PE communications paths.

46. (previously presented): The array processor of claim 45, wherein said cluster switches are further connected to provide direct communications between PEs in a transpose PE pair within a cluster.

47. (previously presented): The array processor of claim 45, wherein said clusters are scaleable.

Please add new claims as follows:

48. (new): An array processor comprising:

a first cluster having a first plurality of processing elements;

a cluster switch, each processing element connected to the cluster switch; and

a cluster control line connected to the cluster switch for carrying a control signal, the control signal controlling the operation of the cluster switch to selectively establish a connection path between two processing elements of the first plurality of processing elements, wherein each connection path established through the cluster switch is communicatively equivalent to a separate wire connection between two processing elements disposed in a torus network.

49. (new): The array processor of claim 48 further comprising:

a second cluster having a second plurality of processing elements, the cluster switch being further operable to establish a connection path between one processing element of the first plurality of processing elements with a processing element of the second plurality of processing elements.

50. (new): The array processor of claim 48 wherein each processing element has an identifier which represents a matrix coordinate for a matrix element of a matrix, the matrix

having a number of matrix elements greater than the number of processing elements in the first cluster.

51. (new): The array processor of claim 50 wherein each processing element of the first plurality of processing elements has a matrix coordinate which is the transpose of another processing element in the first plurality of processing elements or a matrix coordinate having equal indices.

52. (new): The array processor of claim 51 wherein the cluster switch further comprises a first plurality of multiplexers to establish an intra-cluster connection path between two processing elements in the first plurality of processing elements.

53. (new): The array processor of claim 52 wherein the cluster switch further comprises a second plurality of multiplexers for establishing a inter-cluster connection path between a processing element in the first plurality of processing elements and a processing element within an adjacent cluster.

54. (new): An array processor comprising:

a plurality of clusters, each cluster having a plurality of processing elements, each processing element having an identifier which represents a matrix coordinate for a matrix element of a matrix, the matrix having a number of matrix elements greater than the number of processing elements of any cluster;

a plurality of cluster switches, each cluster switch connecting two adjacent clusters, each cluster switch operable to establish a one connection path between processing elements located in the same cluster or between processing elements located in adjacent clusters; and

a plurality of control lines controlling the plurality of cluster switches to select a connection path to establish between processing elements.

55. (new): The array processor of claim 54 wherein the plurality of control lines carry signals to establish connection paths between nearest neighbor processing elements, each established connection path has an input direction and an output direction, the input direction is relative to the matrix coordinate of the processing element receiving input, the output direction is relative to the matrix coordinate of the processing element transmitting output.

56. (new): The array processor of claim 55 wherein the input direction is North, South, East, or West.

57. (new): The array processor of claim 56 wherein the output direction is North, South, East, or West and different from the established input direction.

58. (new): The array processor of claim 54 wherein each processing element of each cluster has a matrix coordinate which is the transpose of another processing element in the same cluster or a matrix coordinate having equal indices.

59. (new): The array processor of claim 58 wherein each processing element's nearest matrix element neighbor is located within the same cluster or in an adjacent cluster.

60. (new): A method of arranging processing elements within a plurality of clusters to perform matrix operations in parallel, the method comprising:

identifying processing elements to represent a matrix coordinate for a matrix element of a matrix, the matrix having a number of matrix elements greater than the number of processing elements in any one cluster;

grouping processing elements into each cluster such that each cluster contains processing elements and their transpose processing elements;

selecting at least two of the processing elements; and

establishing a communication path between the at least two of the processing elements.

61. (new): The method of claim 60 wherein the establishing step further comprises establishing a communication path between two processing elements disposed within the same cluster.

62. (new): The method of claim 60 wherein the establishing step further comprises establishing a communication path between two processing elements disposed in adjacent clusters.